

## *An ultra low-power RFIC chip for wireless and communication applications*

### Motivation

Wearable technology creates the next era of examination and management of the patients. As such, the proposed Body Sensor Networks have the potential to be the next generation of medical equipment. This is the vision of future clinical applications of some physicians. They argue that the use of wearable monitoring devices, which allow continuous or intermittent monitoring of physiological signals, is critical for the advancement of both the diagnosis as well as the treatment. One of the key enabling technologies in order to implement the wearable monitoring devices is the Ultra Low-Power Radio Frequency Integrated Chip (RFIC) Transceiver. This wireless RFIC transceiver is needed for reliable transfer of data for monitoring purposes.

### Objective

To develop a communications subsystem on a chip for Body Sensor Nodes using 2.4GHz ultra low power RF Transceiver.

### Scope

This RFIC Transceiver will have the following key features:

- Ultra low current consumption:  
Receiver/Transmitter/PLL = 5mA/5mA/4mA.
- Ultra low power consumption of about 17mW.
- High Sensitivity of -85dBm.
- Data rates of 250 kbps.
- 16 RF channels.

The task involved will be divided into three portions, namely the design of the receiver, the design of the transceiver and the design of the phase-locked loop (PLL).

### Innovative Ideas

Some ideas to achieve low power and low cost design include:

1. The ultra-low-power system receiver (Fig. 1) will support a data rate of 250 kbps. By performing only a single frequency translation, the need for off-chip filtering is eliminated, allowing for a true System-on-Chip (SoC) design.
2. The system transmitter (Fig. 2) will feature three distinct output power levels, which will optimize the reception under different interference conditions.
3. The Front-End block features a low power, stacked LNA and Mixer. Merging the LNA and Mixer results in a 35% reduction in power consumption, and improves linearity and area efficiency. It has a noise figure of 8 dB at 2 MHz IF, a conversion gain of 17 dB, and an IIP3 above -1 dBm, while drawing only 2 mW from the 1.8 V supply.

## Demonstrable Activities

A fully integrated ultra low power transceiver will be demonstrated. In addition, the performance of each block used in the transceiver design will also be tested and measured. The important parameters that will be measured include the power consumption, noise figure, data rate and number of usable channel.



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### System Overview

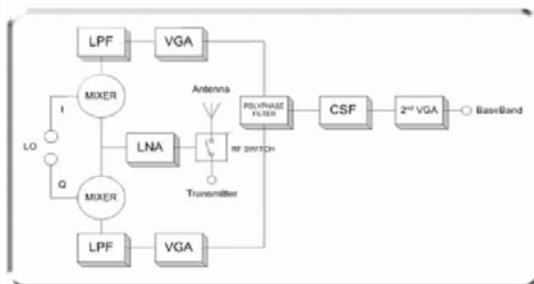


Fig. 1: System Receiver Front End

The ultra-low-power system receiver (Fig. 1) will support a data rate of 250 kbps. By performing only a single frequency translation, the need for off-chip filtering is eliminated, allowing for a true System-on-Chip (SoC) design.

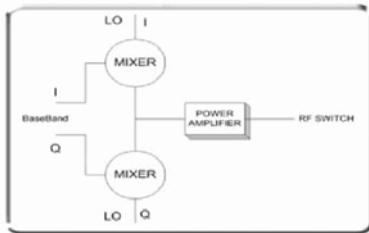
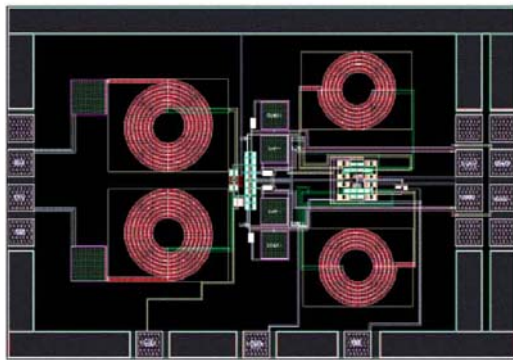


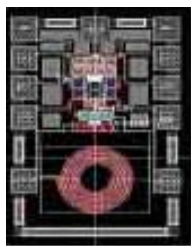
Fig. 2: System Transmitter

The system transmitter (Fig. 2) will feature three distinct output power levels, which will optimize the reception under different interference conditions.

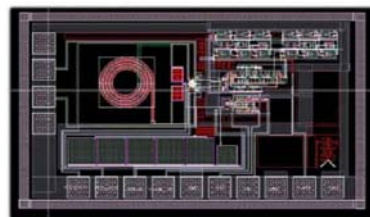


Layout of the stacked LNA and Mixer with test circuit

The Front-End block features a low power, stacked LNA and Mixer. Merging the LNA and Mixer results in a 35% reduction in power consumption, and improves linearity and area efficiency. It has a noise figure of 8 dB at 2 MHz IF, a conversion gain of 17 dB, and an IIP3 above -1 dBm, while drawing only 2 mW from the 1.8 V supply.

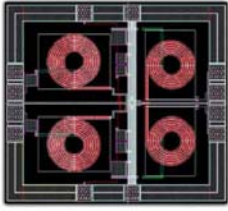


VCO



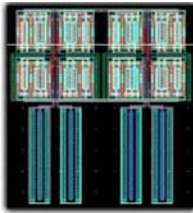
PLL

The quadrature generator provides broadband in-phase and quadrature-phase clock signals. The designed Phase-Locked Loop is optimized for ISM band (2.4 Giga-Hertz) operation and features ultra-low power consumption.



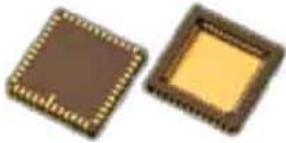
#### PA

The PA has low power consumption and can operate at low supply voltage. It delivers a 1mW RF output for short range application. Multi-level outputs are possible for different situations to optimize power efficiency. Our proposed PA offers excellent linearity, high 1-dB compression point and very good IP3.

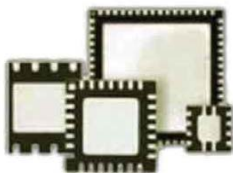


#### QUADRATURE MIXER

This mixer employs passive mode operation for low power consumption. In addition, the proposed mixer has high rejection of spurious signals.



CLCC advantages:  
High reliability/ good hermeticity.  
Small package outline.



Exceptional thermal & electrical performance by design.  
QFN advantages:  
Low inductance. Thin profile & superior die to body size ratio.  
Good thermal & electrical performance